(12) UK Patent Application (19) GB (11) 2 273 009 (13) A

(43) Date of A Publication 01.06.1994

(21) Application No 9224975.4

(22) Date of Filing 28.11.1992

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(51) INT CL[5]
H03G 3/20

(52) UK CL (Edition M)
H3G GPT G10N

(56) Documents Cited
None

(58) Field of Search
UK CL (Edition L) H3G GPT , H3Q QBAX QBQS , H3W WUN , H4L LETXX
INT CL[5] H03F 1/26 , H03G 3/20 3/30 , H04B 7/005

(54) RF Power amplifier ramp control of power level rise and fall

(57) An RF power amplifier is provided having means for defining rise and fall envelopes of the RF power, i.e. the key and de-key characteristics. A power amplifer (10), detector (13) and regulator (15) form a power control feedback loop. A further regulator (21) is provided having a first input coupled to the output of the power control loop regulator and an output coupled to the input of the power control loop regulator, thereby providing negative feedback to the power control loop regulator. Means are provided, coupled to a second input of the further regulator for providing a rising and falling control signal (Vramp) for control of the power amplifier. Use in the transmitter of a mobile communications apparatus is described.

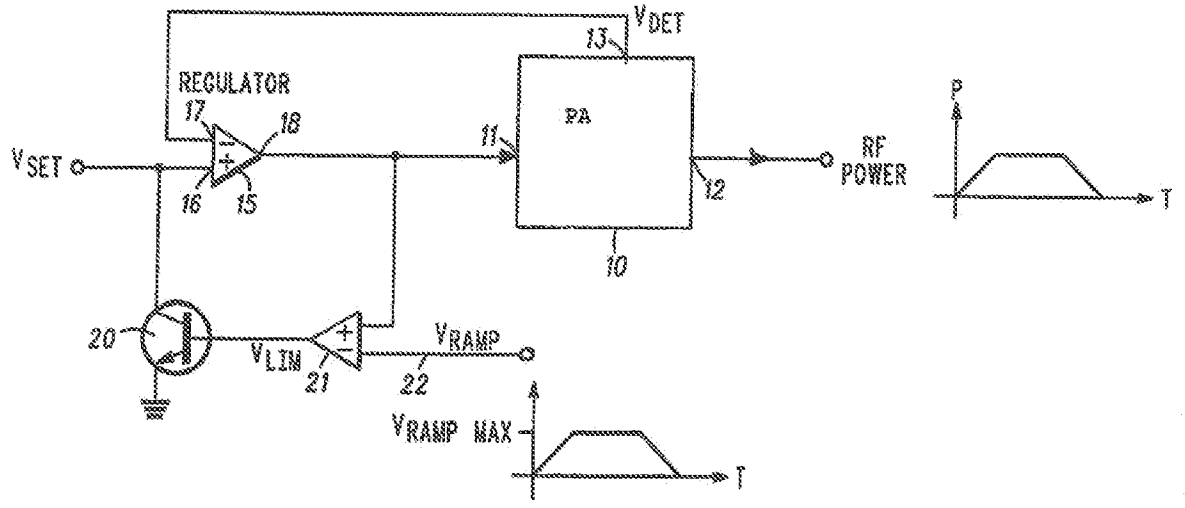

FIG.1

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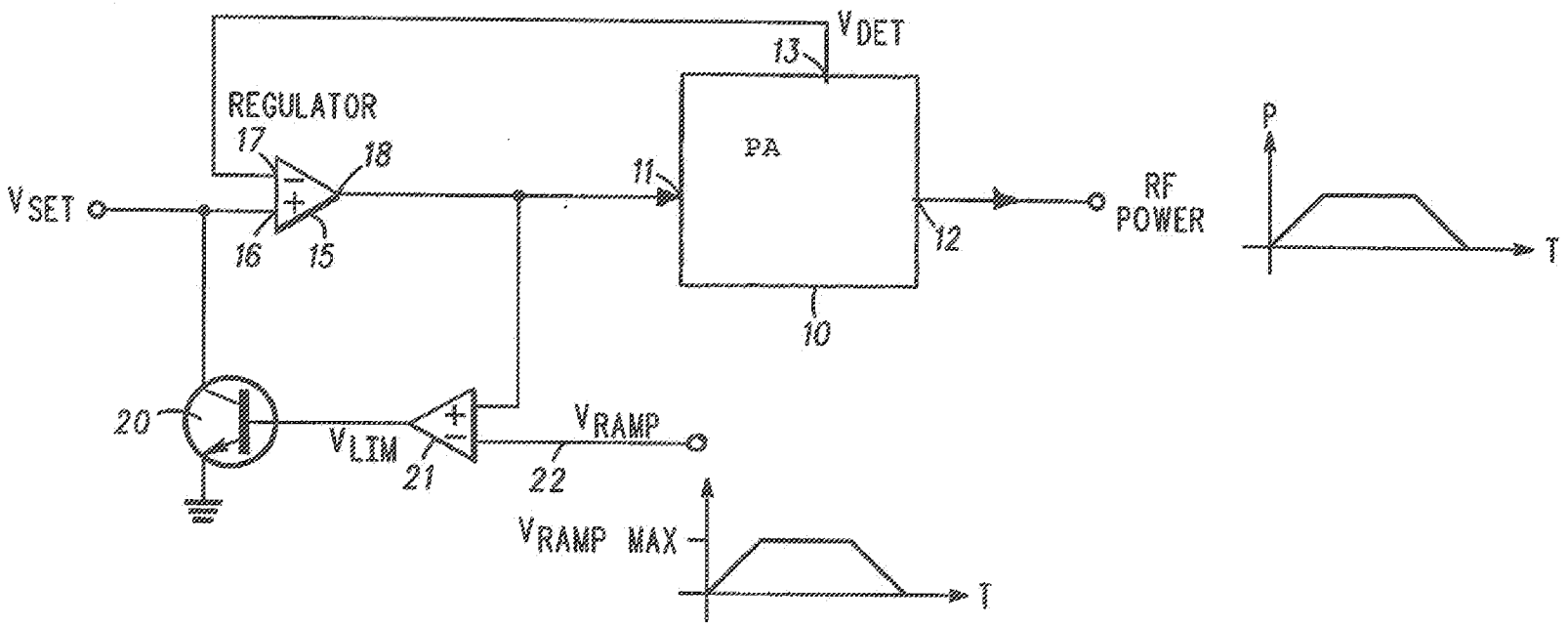
V DET
13
REGULATOR
17
18
V SET
11
PA
RF
POWER
P
16
15
12
T
10
20
V LIM
21
V RAMP
22
V RAMP MAX
T

FIG. 1

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RF POWER AMPLIFIER CONTROL

Field of the Invention

This invention relates to an RF power amplifier having means for defining the rise and fall envelopes of the RF power, i.e. the key and de-key characteristics.

Background to the Invention

Regulatory bodies set out detailed specifications for cyclic keying of radio transmitters, for example in mobile radios, in order to minimise spurious emissions.

International patent application PCT/EP91/00146 describes an arrangement in which a power rise and fall envelope is defined in a read-only memory (ROM) in order to provide a highly controllable rise and fall power envelope. In the arrangement described in that document, there is a control loop in which the output power of the power amplifier is detected in a detector and fed in a feed back loop to one input of a comparator regulator which controls the power amplifier. The other input of the regulator is derived from a digital-to-analog converter, which derives its input from the ROM.

A problem with prior art power control loops arises from the dynamic range of the detector. Typically the amplifier has to be keyed up and down through 60 dB or more of dynamic range and typically a detector has no more than 30 dB of dynamic range capability. This means that until the power amplifier is keyed to within the dynamic range of the detector, the control loop is in effect open circuit. Moreover, the regulator typically requires a high gain in order to achieve satisfactory steady state operation. In the situation of having an effectively open loop circuit with a high gain regulator, the input to the power amplifier rises at a high rate in a virtually uncontrolled manner. This introduces a significant risk of over-swing. In effect, the input has commenced to rise too fast and too far before the output of the power amplifier enters the dynamic range of the detector and the control loop comes into operation.

In prior art arrangements such as that described in PCT/EP91/00146, a capacitor is introduced between the output and

input of the regulator to provide an integration function. This is not always a fully satisfactory arrangement, because if the capacitor is too small there is over-swing and if it is too large there is a tendency to oscillate in the steady state.

There is a need for an improved power amplifier control arrangement.

Summary of the Invention

According to the present invention, a power amplifier circuit for a radio transmitter is provided comprising a power amplifier having a control input and an output, a detector for monitoring the output power of the amplifier and a regulator coupled to the control input of the power amplifier, wherein the detector is coupled to a first input of the regulator, thereby providing a power control feedback loop, and wherein means are provided, coupled to a second input of the regulator for providing a rising and falling control signal for control of the power amplifier, characterised in that a further regulator is provided having a first input coupled to the output of the power control loop regulator and an output coupled to the second input of the power control loop regulator, thereby providing negative feedback to the power control loop regulator and in that the means for providing the rising and falling control signal are coupled to a second input of the further regulator.

The invention has the advantage of providing slope control which controls the power rise and fall without degrading the steady state loop performance. The problems of power overshoot or ringing during key up are avoided.

The arrangement operates down to very low power levels independently of the RF power level detectors sensitivity, because in effect it is not necessary for the power control loop to be closed during key up.

The power level detector's time constant does not influence the power slope. This is especially advantageous at low RF frequencies (low band, mid band), where high value capacitors are required to filter detector DC voltage. The second regulator can be considered to act as a limiter circuit, limiting the rise of the input to the power amplifier to a value provided by the means for providing

the rising and falling control signal. This has an added benefit in that, in the event of failure in the main control loop, for example in the output power detector, a resulting open loop situation does not lead to uncontrolled increase of the power transmitted by the power amplifier.

In a further preferred feature, means are provided for inputting a level signal for defining the steady state level. This level signal can, for example, be supplied to the second input of the power control loop regulator.

It is particularly preferred that the second regulator controls the level of a signal provided to the second input of the power control loop regulator to a limit defined by the level input. This may be achieved, for example, by means of a transistor or equivalent device which gradually and under the control of the second regulator, causes the level setting signal to increase to its maximum on the second input of the first regulator.

The rising and falling signal may be provided by a microprocessor. It is preferred that a microprocessor provides a controlled rising and falling slope for the signal.

A preferred embodiment of the invention will now be described, by way of example only, with reference to the drawing.

Brief Description of the Drawing

Fig. 1 shows an outline circuit diagram of a circuit in accordance with the invention.

Detailed Description of the Preferred Embodiment

An RF power amplifier 10 is shown, which is readily implemented by one skilled in the art. The power amplifier 10 has a control input 11, an RF power output 12 and a detector output 13. The amplifier also has an RF signal input which is not shown. The signal VDET from output 13 is provided by a simple rectifier.

A regulator 15 is provided having positive and negative inputs 16 and 17 and an output 18. The output 18 is connected to the control input of the power amplifier 10. The negative input 17 of the regulator receives its signal from the VDET output 13 of the

power amplifier. Thus, the power amplifier, detector and regulator 15 form a main control loop with negative feedback. The regulator 15 is arranged to provide a gain factor of 1,000 to 10,000.

Connected to the positive input of regulator 15 is a signal VSET. This is provided by a simple potentiometer arrangement and is pre-set in the factory to define the radio maximum power rating, for example 10 watts or 25 watts. It will be appreciated that in particular arrangements, this may be selected by a D/A converter, for example for dynamic power control.

A NPN bipolar transistor 20 is provided having its collector connected to input 16 of regulator 15 and its emitter connected to ground. A second regulator 21 is provided having its positive input connected to the output of regulator 15 and its output connected to the base of transistor 20. Connected to the negative input of regulator 21 is a control signal input 22 which provides the signal VRAMP shown at the lower right hand side of the figure. This signal 22 is provided by a D/A converter from a microprocessor, but could be provided by an analog circuit.

The operation is as follows.

VSET defines the maximum steady state output power for the main control loop comprising power amplifier 10 and regulator 15. When not transmitting, VRAMP is set at zero and the output VLIM of limiter regulator 21 is high, thus holding transistor 20 open and effectively holding input 16 of regulator 15 low. In this state, the power amplifier is effectively closed.

To key up the transmitter, the signal VRAMP is linearly increased. This has the effect of controllably closing transistor 20 and allowing the input 16 of regulator 15 to rise towards VSET. As the output 18 of regulator 15 rises, this signal is fed back to limiter regulator 21 and the positive input of regulator 21 rises, thus counteracting the effect of VRAMP and providing a complete control loop for regulator 15. In this way, the rise of the output of regulator 15 is fully controlled by VRAMP. After about 30 dB of increase in output power from the power amplifier 10, the detector diode enters its operative range and an output is provided on output 13 of amplifier 10. This output is fed backed to negative input 17 of regulator 15 and the main control loop enters operation and provides negative feedback for the regulator 15, while the output of

regulator 15 increases to its steady state position. A steady state is reached when VRAMP reaches maximum and transistor 20 is fully closed, causing the full value of VSET to be input to the positive input of regulator 15. In a steady state condition VRAMP remains at its maximum and control is exerted by the main control loop.

In the steady state condition, if a fault occurs in the main control loop, for example the detector fails and VDET falls to zero, the output of regulator 15 is prevented from rising further, because this would have the effect of causing a fall on VLIM, thereby opening transistor 20 and causing the input on input 16 of regulator 15 to fall. The circuit is thus very robust.

As a modification to the circuit shown in Fig. 1, a capacitor can be provided between the negative input 22 of regulator 21 and the output of that regulator, thereby implementing an integrator function.

Other modifications can be devised by those skilled in the art, such as inversion of the inputs of regulator 21 and inversion of VRAMP signal, together with appropriate substitution of transistor 20.

Claims

1. A power amplifier circuit for a radio transmitter comprising: a power amplifier having a control input and an output; a detector for monitoring the output power of the amplifier and a regulator coupled to the control input of the power amplifier,wherein the detector is coupled to a first input of the regulator, thereby providing a power control feedback loop, and wherein means are provided, coupled to a second input of the regulator for providing a rising and falling control signal for control of the power amplifier, characterised in that

a further regulator is provided having a first input coupled to the output of the power control loop regulator and an output coupled to the second input of the power control loop regulator, thereby providing negative feedback to the power control loop regulator and in that the means for providing the rising and falling control signal are coupled to a second input of the further regulator.

2. An amplifier according to claim 1, further comprising means for inputting a level signal for defining the steady state level.

3. An amplifier according to claim 2, wherein the level signal is supplied to the second input of the power control loop regulator.

4. An amplifier according to claim 1, 2 or 3, wherein the second regulator controls the level of a signal provided to the second input of the power control loop regulator to a limit defined by the level signal.

5. An amplifier according to any one of claims 2, 3 and 4 further comprising means under the control of the second regulator for gradually causing the level signal to increase to its maximum on the second input of the first regulator.

6. An amplifier according to any one of the preceding claims further comprising a microprocessor arranged to define the rising and falling control signal.

7 An amplifier substantially as hereinbefore described with reference to the figure.

Patents Act 1977
Examiner's report to the Comptroller under
Section 17 (The Search Report) — 8 —

Application number

GB 9224975.4

Relevant Technical fields

(i) UK Cl (Edition L) H3G (GPT) H3Q (QBAX, QBQS) H3W (WUN) H4L (LETXX)

(ii) Int Cl (Edition 5) H03G 3/20, 3/30; H03F 1/26; H04B 7/005

Search Examiner

D MIDGLEY

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

10 FEBRUARY 1993

Documents considered relevant following a search in respect of claims 1-6

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

Category	Identity of document and relevant passages -9-	Relevant to claim

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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